REMARKS

Claim Rejections

Claims 1-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,378,015. Claims 1-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pruett et al. (US-6,263,440) in view of Lam et al. (US-5,545,583).

Drawings

It is noted that the Examiner has accepted the drawings in the outstanding Office Action.

New Claims

By this Amendment, Applicant has canceled claims 1-11 and has added new claims 12-20 this application. It is believed that the new claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

The new claims recite a solid state disk module comprising: an IDE interface (1) for connecting the disk module to a main board of a computer; a flash memory controller (3) for controlling data access and specifying an address for data storage; a flash memory array (4) having a plurality of flash memories, the flash memory array being connected to the flash memory controller for saving data; and a power source (2) connected to the flash memory controller and the flash memory array to supply a working voltage.

In another embodiment of the present invention, the flash memory controller is an MX9691 controller. In another embodiment of the present invention, the flash memory controller and the flash memory array is electrically connected to a circuit board (a). In a further embodiment of the present invention the flash memory controller and the flash memory array are enclosed in a casing (b). In another embodiment of the present invention the IDE interface has an extending interface (11).

The cited reference to Pruett et al. teaches a system for tracking and protecting display monitors by reporting their identity that includes a computer (10) having a power supply (17), a power button (21), a first chipset (44), a CPU host bus (42), and a second chipset (52). The second chipset is connected to a PCI bus (50), which is also connected to the CPU host bus and the first chipset.

As noted by the Examiner, on page 4 of the outstanding Office Action, "Pruett does not expressly teach memory array." Further, Pruett et al. teaches a computer (10) having a power supply (17) and states, at col. 5, lines 56-58:

> The power management logic within the second chipset 52 manages switching between computer power states such as off, standby, sleep, suspend and normal operating states.

Pruett et al. teaches a computer having a power supply, and the second chipset having power management logic but, unlike the present invention, does not teach a power source connected to the flash memory controller and the flash memory array to supply a working voltage. Further, Pruett et al. states, at col. 5, lines 34-35:

> Attached to the flash memory interface in the second chipset 52 is a flash memory module or chip 66.

Pruett et al. teaches the flash memory interface being a chip, but unlike the present invention does not teach the flash memory controller being an MX9691 controller. Further, Pruett et al. does not teach the flash memory controller and the flash memory array being electrically connected to a circuit board. Additionally, Pruett et al. does not teach the flash memory controller and the flash memory array being enclosed in a casing. Further, Pruett et al. does not teach the IDE interface having an extending interface.

The cited reference to Lam et al. recites a method of making a semiconductor trench capacitor cell having a buried strap.

Lam et al. states, at col. 2, lines 17-21:

> There exists a continuing demand for semiconductor memory device designs and processes which utilize fewer processing sequences, while at the same time facilitating greater storage capacity and allowing more densely packed memory arrays.

In the background of the invention, Lam et al. states that there is continuing demand for memory arrays, but unlike the present invention does not teach a flash memory array having a plurality of flash memories. Further, Lam et al. does not teach a power source, an IDE interface, or a flash memory controller.

Even if the teachings of Pruett et al. and Lam et al. were combined, as suggested by the Examiner, the resultant combination does not suggest a memory array having a plurality of flash memories, nor a power source connected to the flash memory controller and the flash memory array to supply a working voltage. Further, the combination does not teach a flash memory controller being an MX9691 controller, the flash memory controller and the flash memory array being electrically connected to a circuit board, the flash memory controller and the flash memory array being enclosed in a casing, or the IDE interface having an extending interface.

It is a basic principle of the Unites States Patent Laws that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of the applicant's disclosure to create a hypothetical or fictional combination which allegedly renders a claim obvious unless there is some direction in the selected prior art patents to combine the selected teachings in a matter to negate the patentability of the claimed subject matter.

The Courts have advocated that even if the prior art may be modified, the modification is not obvious unless the prior art suggests the desirability for the modification. For example, in *In re Fritch*, 922 F.2d 1260, 23 USPQ.2d 1780 (Fed. Cir. 1992), the Court held, at page 1783:

> The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

Neither Pruett et al., nor Lam et al. disclose, or suggest a modification of the specifically disclosed structure that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious the new claims 12-20.

Double Patenting

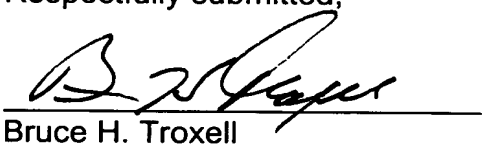
Applicant respectfully traverses the Examiner's rejection of claims 1-11 under the judicially created doctrine of obviousness-type double patenting in view of claims 1-4 of U.S. Patent 6,378,015. It is noted that all of the claims of '015 specifically require a computer having a mother board, and require the memory module to comprise a parallelepiped head housing having at least two edge faces and at least one side face, with a specifically defined area relationship between the at least one side face and at least two edge faces, and an IDE interface connector on a first of the two edge faces engageable with the mother board and also specifically recites a relationship between the interface connector and the mother board. All of the claims of this patent also require a manually operable master/slave switch, and a manually operable read-only switch, as noted in paragraphs d) and g) of claim 1.

The claims of this patent are totally devoid of any recitation of any structure that is even remotely analogous to Applicant's power source connected to the flash memory controller and the flash memory array to supply a working voltage. Applicant notes that there must be some teaching, or suggestion, in the prior art reference that would lead one having ordinary skill in the art to modify the specifically disclosed teachings to arrive at Applicant's claimed invention. Applicant submits that such a teaching or suggestion is totally absent from the cited reference '015. Thus, Applicant submits that new claims 12-20 could not possibly be considered to be obvious in view of claims 1-4 of '015 under 35 U.S.C. § 103. The outstanding rejection of Applicant's claims as being unpatentable over claims 1-4 of '015 is respectfully traversed.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

Date: June 12, 2003 By: 

Bruce H. Troxell
Reg. No. 26,592

TROXELL LAW OFFICE PLLC
5205 Leesburg Pike, Suite 1404
Falls Church, Virginia 22041
Telephone: 703 575-2711
Telefax: 703 575-2707